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MICRO MINUTES

news of MOS microprocessor marketing for the field sales force

$\overline{CE}$ FOR THE MC146818

The chip enable pin ($\overline{CE}$) on the MC146818 may be used for two functions. The first use of this pin is the normal chip select function. The second use of the chip enable line is to isolate the MC146818 from a system which is being powered down, thus preserving the RAM and clock contents. When $\overline{CE}$ is high, all Address/Data (A/D), Data Strobe (DS), Address Strobe (AS), and Read/$\overline{Write}$ (R/$\overline{W}$) are disconnected within the MC146818.

The comparator circuit shown in Figure 1 will trip whenever the unregulated 12V supply falls. Of course, the trip point may be changed to suit individual systems. If only 5 volts is available, the trip point should be set close enough to the reference point to guarantee 2 Address Strobe clocks after the comparator trips (50-200 mV typical) but still allows for system V_{CC} margin. Also, in a +5V system, the reference and sense point will drop during power down. A long time constant on the reference point is recommended.

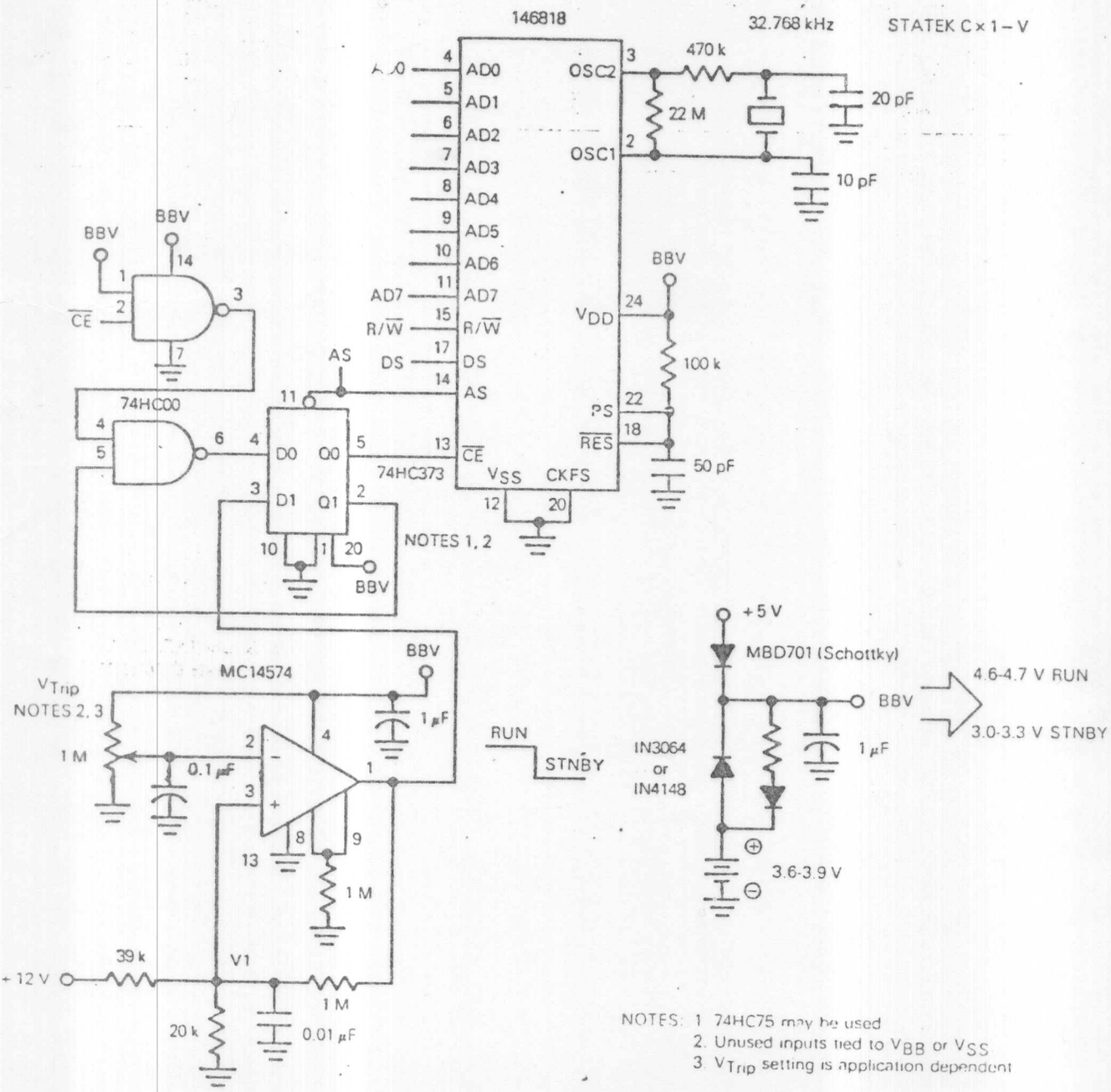
An alternate voltage sensing circuit employing a zener diode is shown in Figure 2. The circuit uses a one (1) volt sense into the base of a NPN transistor. Other supply voltages may be sensed by selecting the appropriate zener diode ($V_{sense} - 1 = V_{zener}$). CMOS MPU's may be directly interfaced with this circuit. If the circuit is used with NMOS MPU's i.e., V_{CC} min. = 4.75V, the sense voltage must be increased to allow for 2 Address Strobes before V_{CC} min. occurs.

Both of these circuits will select or deselect Chip Enable ($\overline{CE}$) during the time Address Strobe (AS) is high, which is required on those units with date code GC6XXXX.

ps

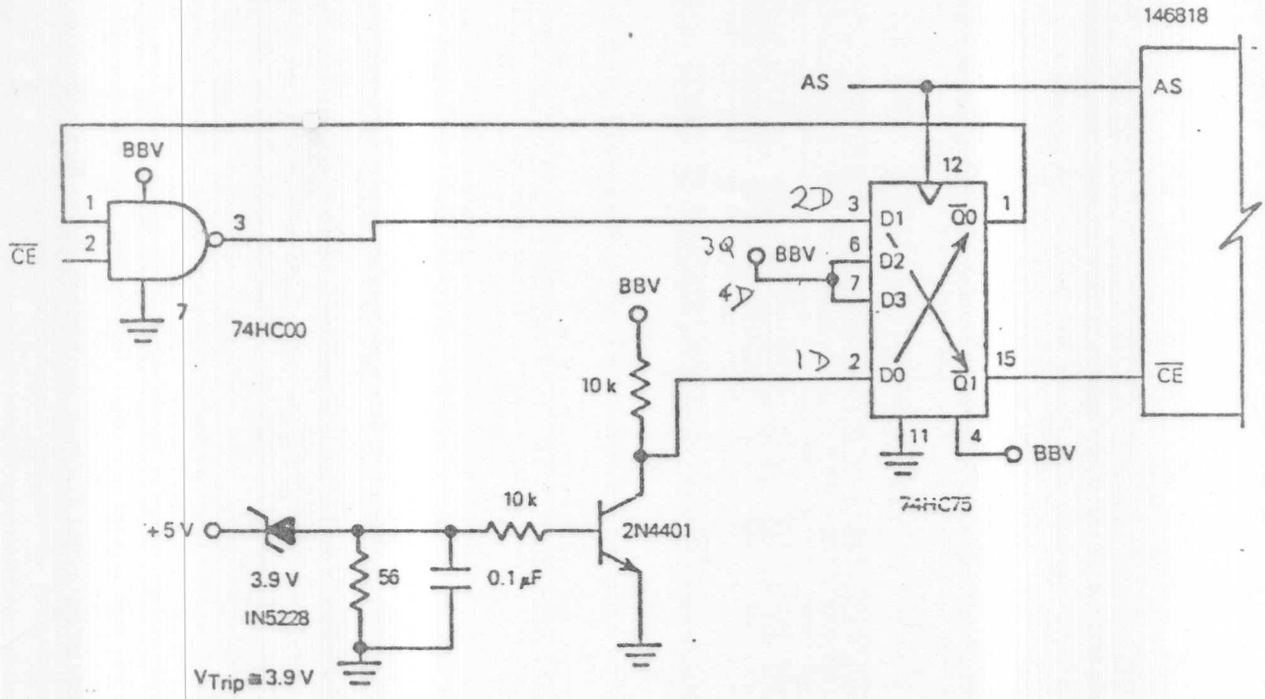
MC146818

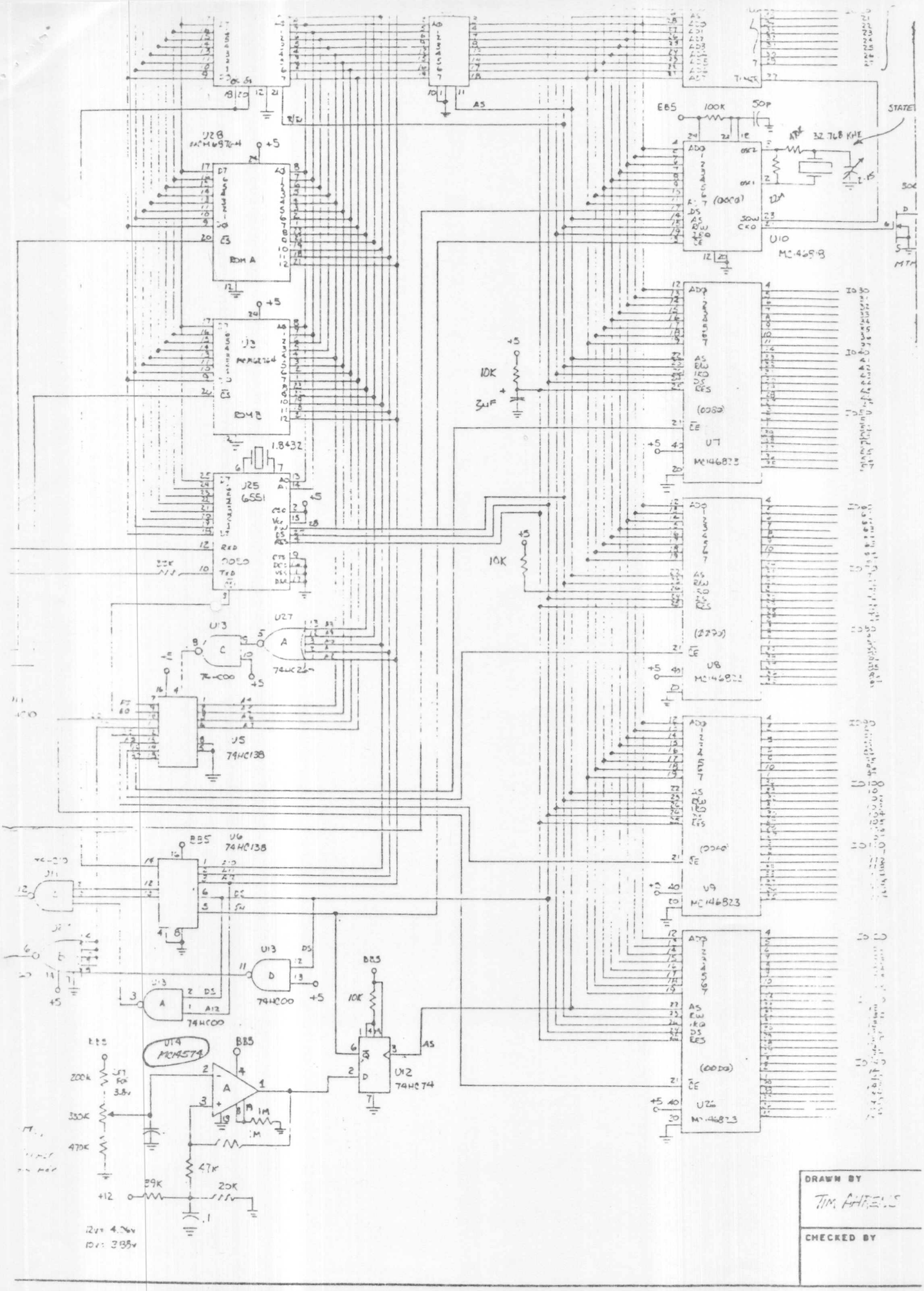
FIGURE 1 — $\overline{CE}$ DURING AS HIGH TIME



NOTES: 1. 74HC75 may be used
2. Unused inputs tied to V_{BB} or V_{SS}
3. V_{Trip} setting is application dependent

FIGURE 2 — $\overline{CE}$ SELECTION AT A.S. HIGH TIME (CMOS MPU's)




U28
MCM6876H
ROM A
U3
MCM6876H
ROM B
1.8432
U25
6551
RXD
TXD
U13
74HC00
U27
74HC259
U5
74HC138
U6
74HC138
U14
MC4574
U12
74HC74
U10
MC146818
U7
MC146823
U8
MC146823
U9
MC146823
U24
MC146823
EB5
100K
50P
STATE1
32.768 KHz
(0000)
(0080)
(2270)
(0040)
(0060)
10K
.1uF
200K
330K
470K
47K
89K
20K
1M
.1
+5
+12
BB5
AS
DRAWN BY
TIM AHRENS
CHECKED BY